Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously presented): A method for operating a microprocessor to reduce power consumption, the microprocessor including a functional unit formed of a plurality of stages, the method comprising:

evaluating instructions to be executed to determine the operation type of each of said instructions, the instructions to be executed depending on operation type by said plurality of stages of said functional unit, where said stages of said functional unit are arranged in series;

producing activity indicators by reading an operation type from an instruction and providing an associated signal comprising one of a clock marker or a no-clock marker based upon the operation types of said instructions;

following said steps of evaluating said instructions and producing said activity indicators, controlling the supply of current to each of said plurality of stages by providing a clock signal and the activity indicators to a logic gate that determines that only selected stages of said plurality of stages will draw current from a power supply, the controlling being based upon activity indicators associated with each of said stages;

advancing said instructions within the microprocessor; and

executing said instructions that are within each of said selected stages.

Claim 2 (original): A method for operating a microprocessor as recited in claim 1 wherein said microprocessor is a very long instruction word processor.

Claim 3 (original): A method for operating a microprocessor as recited in claim 1 wherein the evaluating operates to determine whether each of said instructions is an operation instruction type or a no-operation instruction type.

Claim 4 (original): A method for operating a microprocessor as recited in claim 3 wherein the type of instructions executed in each of said selected stages is an operation instruction type.

Claim 5 (original): A method for operating a microprocessor as recited in claim 3 wherein the producing operates to produce a power-on activity indicator associated with operation instruction types, and a power-off activity indicator associated with no-operation instruction types.

Claim 6 (original): A method for operating a microprocessor as recited in claim 5 wherein said selected stages are associated with power-on activity indicators, and wherein the remaining stages are associated with power-off activity indicators.

Claim 7 (previously presented): A method for operating a microprocessor as recited in claim 1 wherein the controlling operation further comprises:

transmitting the clock signal only to the selected stages of the functional unit.

Claim 8 (previously presented): A method for operating a microprocessor as recited in claim 1 further comprising repeating all of the steps for successive instructions.

Claims 9-16 (cancelled).

Claim 17 (currently amended): A microprocessor that operates in a manner that conserves power, the microprocessor comprising:

an instruction register for temporarily storing a next instruction to be executed;

an instruction evaluation unit that is connected to said instruction register such that said instruction evaluation unit receives said next instruction from said instruction register, said instruction evaluation unit being configured to evaluate said next instruction in order to produce

activity indicators by reading an operation type from the instruction and providing an associated signal comprising one of a clock marker or a no-clock marker based upon the operation types of said instructions;

a functional unit for executing instructions, said functional unit having a plurality of stages, each of said stages capable of being separately activated or deactivated based upon a respective activity indicator, where said stages of said functional unit are arranged in series; ~~and~~

a memory unit for receiving and registering outputs from the functional unit wherein the amount of time required to registering an output comprises time T_r;

a stage activation controller that is connected to said instruction evaluation unit and includes logic gates that utilize said activity indicators in conjunction with a **stage activation controller clock pulse C_{SR}** ~~**stage activation clock pulse of a clock signal**~~ to determine which of said stages are to be activated or deactivated **and wherein the markers are advanced through a shift register of the stage activation controller such that it takes time T_s to advance each marker a shift register in the stage activation controller;**

a clock circuit that supplies a stage activation controller clock pulse C_{SR} to said stage activation controller and also provides a functional unit clock pulse C_{FU} to said functional unit wherein the clock pulse C_{FU} is subject to a gate delay of time T_g, and wherein said functional unit clock pulse C_{FU} is time-delayed with respect to said stage activation controller clock pulse C_{SR} by an amount of time greater than the sum of times T_s, T_r, and T_g thereby enabling the respective stage of the functional unit to have its power status adjusted depending the requirements of the instruction entering said respective stage.

Claim 18 (original): A microprocessor as recited in claim 17 wherein the microprocessor is a very long instruction word processor.

Claim 19 (previously presented): A microprocessor as recited in claim 17 wherein each of said stages have separate inputs for receiving current, the inputs capable of being separately opened or closed, the activated stages having opened inputs and the deactivated inputs having closed inputs.

Claim 20 (original): A microprocessor as recited in claim 17 wherein the stage activation controller is a memory unit that stores said activity indicators.

Claim 21 (original): A microprocessor as recited in claim 20 wherein said memory unit is a register having a bit size equal to the number of stages in said functional unit, each bit location storing a respective activity indicator which indicates whether to activate or deactivate a respective stage.

Claim 22 (original): A microprocessor as recited in claim 17 further comprising a plurality of functional units, each of said functional units having a plurality of stages, each of said stages capable of being separately activated or deactivated based upon a respective activity indicator.

Claim 23 (original): A microprocessor as recited in claim 22 further comprising a plurality of stage activation controllers, each of said stage activation controllers using said activity indicators to individually activate or deactivate each of said stages of a respective one of the plurality of functional units.

Claim 24 (original): A microprocessor as recited in claim 23 further comprising a plurality of instruction evaluation units, each of said instruction evaluation units associated with a respective one of said stage activation controllers.

Claim 25 (previously presented): A microprocessor as recited in claim 17 wherein the logic gates of the stage activation controller comprise AND type gates.

Claims 26-30 (cancelled).

Claim 31 (currently amended): ~~**A microprocessor as recited in claim 26**~~ **A microprocessor that operates in a manner that conserves power, the microprocessor comprising:**

an instruction evaluation unit that evaluates a next instruction to be executed and which produces activity indicators;

a functional unit for executing instructions, said functional unit having a plurality of stages, each of said stages capable of being separately activated or deactivated based upon a respective activity indicator, where said stages of said functional unit are arranged in series;

a stage activation controller that utilizes said activity indicators and causes each of said stages of said functional unit to be individually activated or deactivated stage wherein said stage activation controller is a memory unit that stores said activity indicators;

a clock circuit for supplying clock pulses to each stage of said functional unit and to said stage activation controller; and

an AND gate having an input from said stage activation controller, an input from said clock circuit and an output to one of said stages of said functional unit, whereby said AND gate controls the supply of said clock pulses to said respective.

Claim 32 (original): A microprocessor as recited in claim 31 wherein said memory unit is a register having a bit size equal to the number of stages in said functional unit, each bit location storing a respective activity indicator which indicates whether to activate or deactivate a respective stage.

Claims 33-38 (cancelled).

Claim 39 (previously presented): A method as recited in claim 1 wherein the evaluation and producing steps are performed by an instruction evaluation unit and an instruction register contains the next instruction to be executed, the method further comprising:

receiving said instructions at said instruction evaluation unit from said instruction register; and

receiving said instructions at said functional unit from said instruction register.